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Filing Date	September 30, 2003
First Named Inventor	KIM, Hyunjun.
Art Unit	2841
Examiner Name	Norris, Jeremy C.
Attorney Docket Number	P16828

ENCLOSURES *(Check all that apply)*

- [ ] Fee Transmittal Form
  - [ ] Fee Attached
- [ ] Amendment / Reply
  - [ ] After Final
  - [ ] Affidavits/declaration(s)
- [ ] Extension of Time Request
- [ ] Express Abandonment Request
- [ ] Information Disclosure Statement
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- [ ] Drawing(s)
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- [X] **Appeal Communication to TC (Appeal Notice, Brief, Reply Brief)**
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Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm Name	Buckley, Maschoff & Talwalkar		
Signature	Pat Buckley		
Printed name	Patrick J. Buckley		
Date	June 9, 2006	Reg. No.	40,928

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Signature	Edith Martin		
Typed or printed name	Edith Martin	Date	June 9, 2006

Patent

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: KIM et al.

Application Serial No.: 10/674,886

Filing Date: September 30, 2003

For: FLOATING TRACE ON SIGNAL LAYER

Group Art Unit: 2841

Examiner: Norris, Jeremy C.

Appeal Brief

Attorney Docket No.: P16828

PTO Customer Number 28062
Buckley, Maschoff & Talwalkar LLC
Attorneys for Intel Corporation
Five Elm Street
New Canaan, CT 06840

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Dated: June 9, 2006 By: _____
Edith Martin

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicants hereby submit an appeal to the Board of Patent Appeals and Interferences from the decision of the Examiner in the Final Office Action mailed January 11, 2006 (the "Final Office Action") rejecting claims 1-5, 7-16, and 18-21.

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REAL PARTY IN INTEREST

The present application is assigned to INTEL CORPORATION, 2200 Mission College Blvd, Santa Clara, CA 95052.

RELATED APPEALS AND INTERFERENCES

No other appeals or interferences are known to Applicants or Applicants' legal representative which will directly affect, be directly affected by, or have a bearing on the Board's decision in the pending appeal. The present application has not been assigned to any other party.

STATUS OF CLAIMS

Claims 6 and 17 have been canceled.

Claims 1-5, 7-16, and 18-21 are being appealed.

STATUS OF AMENDMENTS

No amendments have been filed subsequent to the Final Office Action.

SUMMARY OF THE CLAIMED SUBJECT MATTER

A printed circuit board may have a "signal layer" with signal traces (e.g., conductive paths) that electrically connect components, such as processors and other integrated circuits. The printed circuit board may also have one or more voltage planes, such as a power plane and a ground plane, to provide power to the components. In some cases, electromagnetic resonance between voltage planes (e.g., between a power plane and a ground plane) may increase the impedance associated with a printed circuit board. Page 2, lines 2-10.

To improve impedance characteristics, a first conducting portion to be at a first voltage may be provided as a first voltage plane. For example, FIG. 2 illustrates a printed circuit board 200 having a first voltage plane 220 (*e.g.*, a layer of the circuit board dedicated to a power plane). Moreover, a signal layer with signal traces (the top surface of FIG. 2) may be provided on one side of the first voltage plane 220 and a second voltage plane 230 (e.g., a layer of the

circuit board dedicated to ground) may be provided on the other side of the first voltage plane 220. According to some embodiments, a plurality of "floating" microstrip line traces 540 are formed on the signal layer. As illustrated in FIGS. 2 and 3, each microstrip line may be (i) electrically connected to the second conducting portion 530 at a first end, (ii) not directly connected to any other microstrip line at a second end opposite the first end, and (iii) not directly connected to the second conducting portion 530 at the second end.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 1-5, 7-16, and 18-21 are rejected under 35 USC 103 as being unpatentable over US Patent No. 6,172,305 ("Tanahashi").

ARGUMENT

The pending claims recite "a first voltage plane" and "a second voltage plane."

According to the Final Office Action, Tanahashi discloses in FIGS. 3A through 3C: a first voltage plane (12, including P2) and a second voltage plane (11, including G1).

While P2 is a conductor that can be held to a pre-determined voltage level, neither P2 nor layer 12 is a voltage "plane." That is, neither P2 nor layer 12 is a layer of the circuit board dedicated to a voltage level (*e.g.*, a ground plane or a +5.0 volt plane). Indeed, in addition to P2, layer 12 includes ground G2 (see FIG. 3C of Tanahashi).

Similarly, layer 11 is not a voltage plane. Instead, in addition to G1 this layer 11 of the circuit board includes power level P1 and even a signal line S1 (see FIG. 3C of Tanahashi). Thus, layer 12 cannot be considered a "voltage plane" as recited in the claims.

Tanahashi merely discloses that a multi-layer circuit board may be provided (and each layer can have various combinations of ground portions, power portions, and signal portions).

Moreover, the claims recite a "plurality" of floating microstrip line traces on the signal layer. According to page 3 of the Final Office Action, Tanahashi refers to such a feature here:

> Further, a plurality of wiring conductors may be placed for each kind, and various multilayer circuit boards configured by the first to four insulating layers I1 to I4 may be combined and overlaid on the multiplayer circuit board configured by the first to fourth insulating layers I1 to I3.

Tanahashi at column 16, lines 55 to 50. Applicants respectfully suggest that this sentence refers to additional layers being added to the circuit board and does not disclose or suggest that a plurality of floating microstrip lines may be provided on the signal layer as recited in the claims.

Because Tanahashi fails to disclose or suggest these elements, Applicants respectfully request that these rejections be reversed.

Nor would the use of multiple floating traces and voltage planes as recited in the claims be obvious in view of Tanahashi. By configuring the floating traces and voltage planes as recited in the claims, an overall impedance associated with a circuit board may be damped and the efficiency of the power delivery system may be improved (specification of the present application at page 4, lines 7 to 14).

In rejecting claims under 35 U.S.C. § 103, the Examiner bears the initial burden of presenting a *prima facie* case of obviousness. See In re Rijckaert, 9 F.3d 1531, 1532, 28 USPQ2d 1955, 1956 (Fed. Cir. 1993). A *prima facie* case of obviousness is established by presenting evidence that would have led one of ordinary skill in the art to arrive at the claimed invention.

The teaching or suggestion to make the claimed combination must be found in the prior art, and not based on the Applicants' disclosure. In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). "To support the conclusion that the claimed invention is directed to obvious subject matter, either the references must expressly or impliedly suggest the claimed invention or the examiner must present a convincing line of reasoning as to why the artisan would have found the claimed invention to have been obvious in light of the teachings of the references." Ex parte Clapp, 227 USPQ 972, 973 (Bd. Pat. App. & Inter. 1985). The fact that references can potentially be modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. MPEP 2143.01; Monarch Knitting Machinery Corp. v. Sulzer Morat GmbH, 45 USPQ 2d 1977, 1981-82 (Fed. Cir. 1998) (the question to be asked is "whether the prior art contains a suggestion or motivation to combine references").

The absence of any motivation in the prior art (and the lack of a convincing line of reasoning) to configure a plurality of floating traces and voltage planes as recited in the pending claims indicates that the Examiner has simply recognized a benefit provided by the present

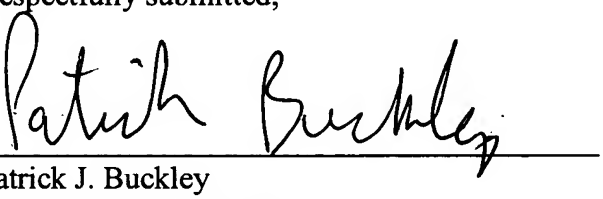
invention, and then used that benefit as a motivation to combine the references – the essence of impermissible hindsight reconstruction.

Because there is no teaching or suggestion to modify the references in this way, a *prima facie* case of obviousness has not been established. The rejection of these claims should be reversed.

CONCLUSION

Applicants respectfully suggest that rejections of claims 1-5, 7-16, and 18-21 are improper and request that the rejections be reversed. If any issues remain, or if the Examiner has any further suggestions for expediting allowance of the present application, the Examiner is kindly invited to contact the undersigned.

Respectfully submitted,



June 9, 2006
Date

Patrick J. Buckley
Registration No. 40,928
Buckley, Maschoff & Talwalkar LLC
Attorneys for Intel Corporation
Five Elm Street
New Canaan, CT 06840

Appendix A - Claims
Appendix B - Evidence
Appendix C - Related Proceedings

APPENDIX A - CLAIMS

This is a complete copy of the claims involved in the appeal:

1. An apparatus, comprising:

a first voltage plane having a first conducting portion to be at a first voltage;

a signal layer on one side of the first voltage plane;

a second voltage plane on the other side of the first voltage plane and having a second conducting portion to be at a second voltage; and

a plurality of floating microstrip line traces on the signal layer, wherein each microstrip line is (i) electrically connected to the second conducting portion at a first end, (ii) not directly connected to any other microstrip line at a second end opposite the first end, and (iii) not directly connected to the second conducting portion at the second end.

2. The apparatus of claim 1, wherein the first voltage plane is a power plane and the second voltage plane is a ground plane.

3. The apparatus of claim 1, wherein the first voltage plane is a ground plane and the second voltage plane is a power plane.

4. The apparatus of claim 1, wherein each microstrip line is substantially 15 μm thick.

5. The apparatus of claim 1, wherein the microstrip line and the second voltage plane are electrically connected via a plated through hole.

6. (canceled)

7. The apparatus of claim 1, wherein the microstrip line provides impedance damping.

8. The apparatus of claim 1, wherein the microstrip line reduces resonance between the first voltage plane and the second voltage plane.

9. The apparatus of claim 1, wherein the first voltage plane, the signal layer, and the second voltage plane are separated by dielectric material.

10. The apparatus of claim 1, wherein the apparatus is a printed circuit board and the microstrip lines are positioned substantially around the perimeter of the board.

11. The apparatus of claim 10, wherein the printed circuit board is associated with at least one of: (i) a flip chip ball grid array package model, and (ii) a pin grid array package model.

12. The apparatus of claim 1, further comprising:

a second signal layer.

13. The apparatus of claim 12, further comprising:

a second plurality of floating microstrip line traces on the second signal layer, wherein each microstrip line in the second plurality is (i) electrically connected to the second voltage plane at a first end, (ii) not directly connected to any other microstrip line at a second end opposite the first end, and (iii) not directly connected to the second voltage plane at the second end.

14. A method, comprising:

providing a first voltage plane having a first conducting portion to be at a first voltage;

providing a signal layer on one side of the first voltage plane;

providing a second voltage plane on the other side of the first voltage plane and having a second conducting portion to be at a second voltage; and

providing a plurality of floating microstrip line traces on the signal layer, wherein each microstrip line is (i) electrically connected to the second voltage plane at a first end, such that each microstrip line is to be at the second voltage, (ii) not directly connected to any other microstrip line at a second end opposite the first end, and (iii) not directly connected to the second conducting portion at the second end.

15. The method of claim 14, further comprising:

positioning the floating trace in the signal layer to reduce cross-talk with a neighboring signal line.

16. The method of claim 14, further comprising:

providing a second signal layer; and

providing a second plurality of floating microstrip line traces on the second signal layer, wherein each microstrip line in the second plurality is (i) electrically connected to the second voltage plane at a first end, (ii) not directly connected to any other microstrip line at a second end opposite the first end, and (iii) not directly connected to the second voltage plane at the second end.

17. (canceled)

18. A printed circuit board, comprising:

a signal layer including a plurality of microstrip lines that are not electrically connected to each other on the signal layer;

a power plane under the signal layer and separated from the signal layer by a dielectric material, the power plane having a power conducting portion to be at a power voltage; and

a ground plane under the power plane and separated from the power plane by the dielectric material, the ground plane having a ground conducting portion to be at a ground voltage,

wherein each of the microstrip lines is (i) electrically connected to the ground conducting portion via a plated through hole passing through the dielectric material and the power plane at a first end, (ii) not directly connected to other microstrip lines on the signal layer, and (iii) not directly connected to the ground conducting portion at a second end opposite the first end.

19. The printed circuit board of claim 18, wherein the microstrip lines provide impedance damping and reduce resonance between the power plane and the ground plane.

20. A system, comprising:

a printed circuit board, including:

a first voltage plane having a first conducting portion to be at a first voltage,

a signal layer on one side of the first voltage plane,

a second voltage plane on the other side of the first voltage plane and having a first conducting portion to be at a first voltage, and

a plurality of floating microstrip line traces on the signal layer, wherein each microstrip line is (i) electrically connected to the second conducting portion at a first end, (ii) not directly connected to any other microstrip line at a second end opposite the first end, and (iii) not directly connected to the second conducting portion at the second end; and

a dynamic random access memory unit coupled to the printed circuit board.

21. The system of claim 20, further comprising:

a processor coupled to the printed circuit board, wherein the processor and dynamic random access memory unit are to exchange information via signal lines on the signal layer.

APPENDIX B - EVIDENCE

No evidence is submitted herewith (*i.e.*, this appendix is empty).

APPENDIX C - RELATED PROCEEDINGS

No other appeals or interferences are known to Applicants or Applicants' legal representative which will directly affect, be directly affected by, or have a bearing on the Board's decision in the pending appeal. The present application has not been assigned to any other party.

Therefore, there are no copies of decisions rendered by a court or the Board to attach (*i.e.*, this appendix is empty).